What is claimed is:

[Claim 1] 1. A thin film transistor array substrate having a pixel region and a peripheral region surrounding the pixel region, comprising:

a transparent substrate;

a thin film transistor array, disposed over the transparent substrate within the pixel region, wherein the thin film transistor array at least comprises a first conductive layer and a second conductive layer;

a plurality of first lead lines, disposed over the transparent substrate within the peripheral region, wherein both the first lead lines and the first conductive layer belong to a same film layer;

a plurality of second lead lines, disposed over the transparent substrate within the peripheral region, wherein both the second lead lines and the second conductive layer belong to a same film layer; and

a first shielding layer, disposed over the transparent substrate within the peripheral region to cover the gaps between neighboring first lead lines, and both the first shielding layer and the second conductive layer belong to a same film layer.

[Claim 2] 2. The thin film transistor array substrate of claim 1, further comprising a second shielding layer disposed over the transparent substrate within the peripheral region to cover the gaps between neighboring second lead lines, and both the second shielding layer and the first conductive layer belong to the same film layer.

[Claim 3] 3. The thin film transistor array substrate of claim 2, wherein a common voltage is applied to the first shielding layer.

[Claim 4] 4. The thin film transistor array substrate of claim 3, wherein a common voltage is applied to the second shielding layer.

[Claim 5] 5. The thin film transistor array substrate of claim 1, wherein a common voltage is applied to the first shielding layer.

[Claim 6] 6. The thin film transistor array substrate of claim 1, wherein the first conductive layer comprises a gate layer, and the second conductive layer comprises a source/drain layer.

[Claim 7] 7. The thin film transistor array substrate of claim 1, wherein the first conductive layer comprises a source/drain layer, and the second conductive layer comprises a gate layer.

[Claim 8] 8. A thin film transistor array substrate having a pixel region and a peripheral region surrounding the pixel region, comprising:

a transparent substrate;
a thin film transistor array, disposed over the transparent substrate within the pixel region, wherein the thin film transistor array at least comprises a first conductive layer and a second conductive layer;
a plurality of first lead lines, disposed over the transparent substrate within the peripheral region, wherein the first lead lines and the first conductive layer belong to a same film layer;
a plurality of first bonding pads, disposed over the transparent substrate within the peripheral region and connected to the first lead lines, wherein the first bonding pads and the first conductive layer belongs to the same film layer;
a plurality of second lead lines, disposed on the transparent substrate within the peripheral region, wherein the second lead lines and the second conductive layer belong to a same film layer;
a plurality of second bonding pads, disposed on the transparent substrate within the peripheral region and connected to the second lead lines, wherein the second bonding pads and the second conductive layer belong to a same film layer; and
a first shielding layer, disposed on the transparent substrate within the peripheral region to cover the gaps between neighboring first lead lines, wherein the first shielding layer and the second conductive layer belong to a same film layer.

[Claim 9] 9. The thin film transistor array substrate of claim 8, further comprising a second shielding layer disposed over the transparent substrate within the peripheral region to cover the gaps between neighboring second lead lines, and the second shielding layer and the first conductive layer belong to the same film layer.

[Claim 10] 10. The thin film transistor array substrate of claim 9, wherein a common voltage is applied to the first shielding layer.

[Claim 11] 11. The thin film transistor array substrate of claim 10, wherein a common voltage is applied to the second shielding layer.

[Claim 12] 12. The thin film transistor array substrate of claim 8, wherein a common voltage is applied to the first shielding layer.

[Claim 13] 13. The thin film transistor array substrate of claim 8, wherein the first conductive layer comprises a gate layer, and the second conductive layer comprises a source/drain layer.

[Claim 14] 14. The thin film transistor array substrate of claim 8, wherein the first conductive layer comprises a source/drain layer, and the second conductive layer comprises a gate layer.

[Claim 15] 15. A method of fabricating a thin film transistor array substrate, comprising the steps of:

providing a transparent substrate, wherein the transparent substrate comprises a pixel region and a peripheral region;

forming a patterned gate layer over the transparent substrate within the pixel region and a plurality of first lead lines and a plurality of first bonding pads connected to the first lead lines on the transparent substrate within the peripheral region;

forming an insulating layer over the transparent substrate covering the gate layer and the first lead lines;

forming a patterned channel layer over the insulating layer above the gate layer; and

forming a patterned source/drain layer over the channel layer and a plurality of second lead lines and a plurality of second bonding pads connected to the second lead lines over the transparent substrate within the peripheral region; wherein a first shielding layer formed to cover the gaps between neighboring first lead lines.

[Claim 16] 16. The method of fabricating a thin film transistor array substrate of claim 15, wherein the first shielding layer further extends to cover the gaps between neighboring first bonding pads.

[Claim 17] 17. The method of fabricating a thin film transistor array substrate of claim 15, wherein the step of forming the gate layer further comprises a step of forming a second shielding layer under the gaps between subsequently formed neighboring second lead lines.

[Claim 18] 18. The method of fabricating the thin film transistor array substrate of claim 17, wherein the step of forming the second shielding layer further comprises a step of extending the second shielding layer into an region under the gaps between subsequently formed neighboring second bonding pads.

[Claim 19] 19. A method of fabricating a thin film transistor array substrate, comprising the steps of:

providing a transparent substrate, wherein the transparent substrate includes a pixel region and a peripheral region;
forming a patterned gate layer over the transparent substrate within the pixel region and a plurality of first lead lines and a plurality of first bonding pads connected to the first lead lines on the transparent substrate within the peripheral region;
forming an insulating layer over the transparent substrate covering the gate layer and the first lead lines;
forming a patterned channel layer over the insulating layer above the gate layer; and
forming a patterned source/drain layer over the channel layer and a plurality of second lead lines and a plurality of second bonding pads connected to the second lead lines over the transparent substrate within the peripheral region;
wherein a shielding layer is formed under the gaps between subsequently formed neighboring second lead lines.

[Claim 20] 20. The method of fabricating the thin film transistor array substrate of claim 19, wherein the step of forming the

shielding layer further comprises a step of extending the shielding layer into an region under the gaps between subsequently formed neighboring second bonding pads.